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Driver v. 5.01

Moreno Ortolan

Interfacing FlashRunner 2.0 with TELECHIPS TCC

SMH Technologies S.r.l.

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TELECHIPS TCC Introduction

TCC7x with Arm Cortex-R5 MCUs

Wireless Charger, Cluster, Telematics, CID and IVI

TCC70xx (VCP) Family of 32-bit automotive microcontrollers (MCUs) offers a solution for various automotive applications designed for Wireless Charger, Cluster, Telematics, CID and IVI with very low power consumption over a wide and scalable range of products from 2 to 4MB flash / 256 to 512KB RAM based the Arm® Cortex®-R5 Floating Point CPU, which includes a security sub-system based on Arm Cortex-M0.

TCC70xx (VCP) Family is offered in a Samsung 28nm process, a World's first qualified 28nm (12" Wafer), and have advanced security features with the introduction of EVITA Full HSM (Hardware security module), dedicated Cortex®-M0 for secure processing, also qualified AEC-Q100 with advanced safety and software support for industrial and automotive ASIL-B applications.

TCC70xx (VCP) Family provides Giga-bit Ethernet backbone for better performance, safe and efficient automotive communication along with global trends which require high-speed interface. Furthermore, it supports up to 125°C ambient, CAN, LIN, UART, CSI, I2C interfaces and hard- & software compatibility across family, as well as Inter-IC Sound (I2S) Interfaces implemented for connecting digital audio devices.

MCU:
(Wireless Charger, Cluster, Telematics, CID, IVI)

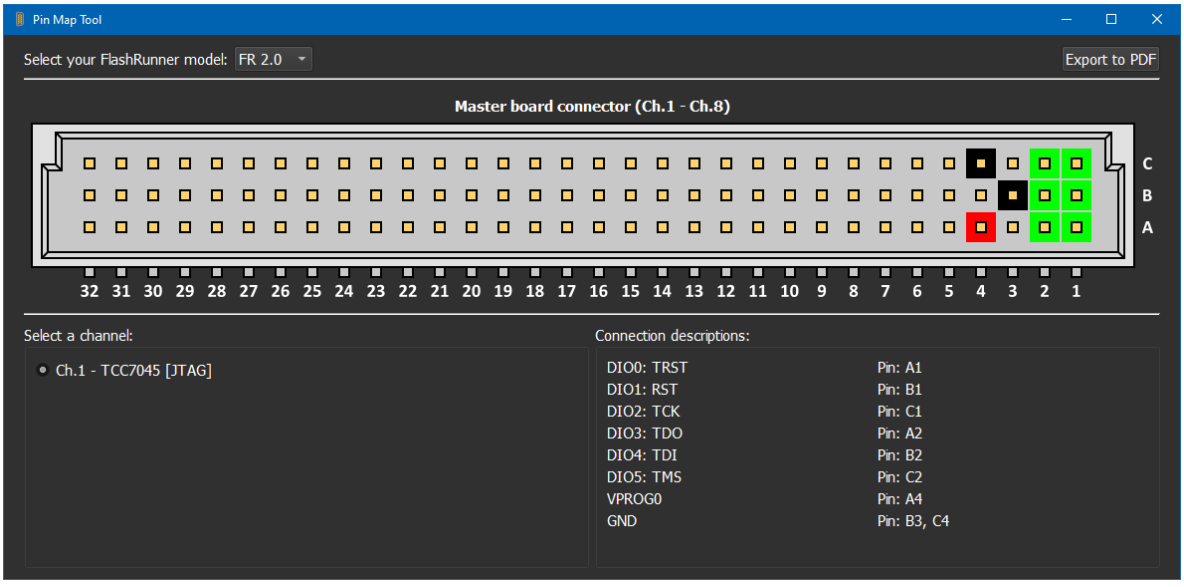
- **TCC7022 (VCP-22)**
- **TCC7025 (VCP-25)**
- **TCC7035 (VCP-35)**
- **TCC7045 (VCP-45)**

TELECHIPS TCC Protocol and PIN map

TCC7x devices support the JTAG protocol.

```
#TCSETPAR CMODE <JTAG>
```

TELECHIPS TCC PIN MAP



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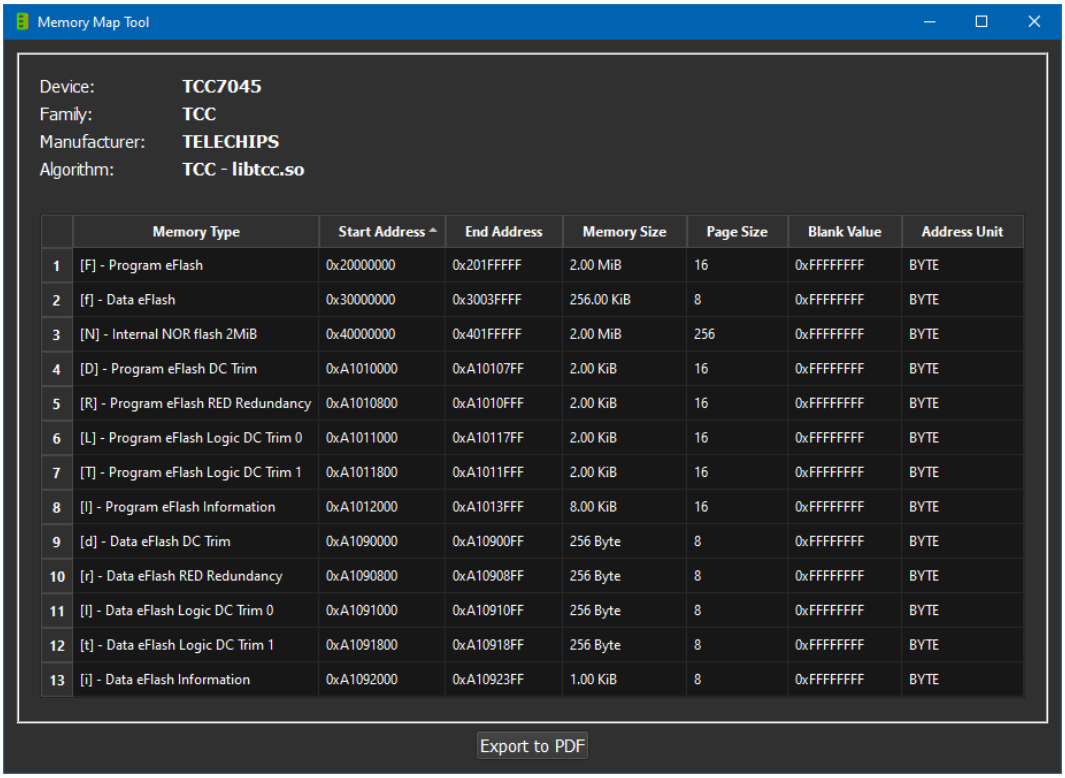
TELECHIPS TCC Memory Map

Memory Type	Start Address	End Address	Memory Size	Page Size	Blank Value	Address Unit
[F] - Program eFlash	0x20000000	0x201FFFFF	2.00 MiB	16	0xFFFFFFFF	BYTE
[f] - Data eFlash	0x30000000	0x3003FFFF	256.00 KiB	8	0xFFFFFFFF	BYTE
[N] - Internal NOR flash 2MiB	0x40000000	0x401FFFFF	2.00 MiB	256	0xFFFFFFFF	BYTE
[D] - Program eFlash DC Trim	0xA1010000	0xA10107FF	2.00 KiB	16	0xFFFFFFFF	BYTE
[R] - Program eFlash RED Redundancy	0xA1010800	0xA1010FFF	2.00 KiB	16	0xFFFFFFFF	BYTE
[L] - Program eFlash Logic DC Trim 0	0xA1011000	0xA10117FF	2.00 KiB	16	0xFFFFFFFF	BYTE
[T] - Program eFlash Logic DC Trim 1	0xA1011800	0xA1011FFF	2.00 KiB	16	0xFFFFFFFF	BYTE
[I] - Program eFlash Information	0xA1012000	0xA1013FFF	8.00 KiB	16	0xFFFFFFFF	BYTE
[d] - Data eFlash DC Trim	0xA1090000	0xA10900FF	256 Byte	8	0xFFFFFFFF	BYTE
[r] - Data eFlash RED Redundancy	0xA1090800	0xA10908FF	256 Byte	8	0xFFFFFFFF	BYTE
[l] - Data eFlash Logic DC Trim 0	0xA1091000	0xA10910FF	256 Byte	8	0xFFFFFFFF	BYTE
[t] - Data eFlash Logic DC Trim 1	0xA1091800	0xA10918FF	256 Byte	8	0xFFFFFFFF	BYTE
[i] - Data eFlash Information	0xA1092000	0xA10923FF	1.00 KiB	8	0xFFFFFFFF	BYTE



	Memory Type	Start Address	End Address	Memory Size	Page Size	Blank Value	Address Unit
1	[F] - Program eFlash	0x20000000	0x201FFFFF	2.00 MiB	16	0xFFFFFFFF	BYTE
2	[f] - Data eFlash	0x30000000	0x3003FFFF	256.00 KiB	8	0xFFFFFFFF	BYTE
3	[N] - Internal NOR flash 2MiB	0x40000000	0x401FFFFF	2.00 MiB	256	0xFFFFFFFF	BYTE
4	[D] - Program eFlash DC Trim	0xA1010000	0xA10107FF	2.00 KiB	16	0xFFFFFFFF	BYTE
5	[R] - Program eFlash RED Redundancy	0xA1010800	0xA1010FFF	2.00 KiB	16	0xFFFFFFFF	BYTE
6	[L] - Program eFlash Logic DC Trim 0	0xA1011000	0xA10117FF	2.00 KiB	16	0xFFFFFFFF	BYTE
7	[T] - Program eFlash Logic DC Trim 1	0xA1011800	0xA1011FFF	2.00 KiB	16	0xFFFFFFFF	BYTE
8	[I] - Program eFlash Information	0xA1012000	0xA1013FFF	8.00 KiB	16	0xFFFFFFFF	BYTE
9	[d] - Data eFlash DC Trim	0xA1090000	0xA10900FF	256 Byte	8	0xFFFFFFFF	BYTE
10	[r] - Data eFlash RED Redundancy	0xA1090800	0xA10908FF	256 Byte	8	0xFFFFFFFF	BYTE
11	[l] - Data eFlash Logic DC Trim 0	0xA1091000	0xA10910FF	256 Byte	8	0xFFFFFFFF	BYTE
12	[t] - Data eFlash Logic DC Trim 1	0xA1091800	0xA10918FF	256 Byte	8	0xFFFFFFFF	BYTE
13	[i] - Data eFlash Information	0xA1092000	0xA10923FF	1.00 KiB	8	0xFFFFFFFF	BYTE

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TELECHIPS TCC Driver Parameters

The standard parameters are used to configure some specific options inside TCC driver.

#TCSETPAR ENTRY_CLOCK

Syntax: **#TCSETPAR** ENTRY_CLOCK <Frequency>

<Frequency> Accepted parameters 4000000, 2000000, 1000000, 500000, 100000 Hz

Description: Set the JTAG frequency used in the Connect procedure before raising the PLL of the device, if the device PLL is available

Note: Default value 4.00 MHz

#TCSETPAR QSPI_FREQUENCY

Syntax: **#TCSETPAR** QSPI_FREQUENCY <Value>

<Value> Accepted parameter is 85MHz

Description: Set the SFMC0 frequency for SPI peripheral

Note: Default value 85MHz
Available only for **TCC7035** and **TCC7045**

#TCSETPAR QSPI_PROTOCOL

Syntax: **#TCSETPAR** QSPI_PROTOCOL <Value>

<Value> Accepted parameters are:

- QUAD-SPI
- EXTENDED-SPI
- SPI

Description: Set the SFMC0 protocol used to communicate with SNOR memory

Note: Default value QUAD-SPI
Available only for **TCC7035** and **TCC7045**

#TCSETPAR INTERNAL_MEMORY_QSPI_FREQUENCY

Syntax: **#TCSETPAR** INTERNAL_MEMORY_QSPI_FREQUENCY <Value>

<Value> Accepted parameter are:

- 100MHz
- 90MHz
- 80MHz
- 70MHz
- 60MHz
- 50MHz
- 40MHz
- 30MHz
- 20MHz
- 10MHz

Description: Set the SFMC0 frequency for SPI peripheral

Note: Default value 85MHz
Available only for **TCC7035** and **TCC7045**
Available from driver version **5.01**

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#TCSETPAR INTERNAL_MEMORY_QSPI_PROTOCOL

Syntax: **#TCSETPAR** INTERNAL_MEMORY_QSPI_PROTOCOL <Value>

<Value> Accepted parameters are:
- QUAD-SPI
- EXTENDED-SPI
- SPI

Description: Set the SFMC0 protocol used to communicate with SNOR internal memory

Note: Default value QUAD-SPI
Available only for **TCC7035** and **TCC7045**
Available from driver version **5.01**

#TCSETPAR EXTERNAL_MEMORY_QSPI_FREQUENCY

Syntax: **#TCSETPAR** EXTERNAL_MEMORY_QSPI_FREQUENCY <Value>

<Value> Accepted parameter are:
- 50MHz
- 45MHz
- 40MHz
- 35MHz
- 30MHz
- 25MHz
- 20MHz
- 15MHz
- 10MHz
- 5MHz

Description: Set the SFMC1 frequency for SPI peripheral

Note: Default value 50MHz
Available from driver version **5.01**

#TCSETPAR EXTERNAL_MEMORY_QSPI_PROTOCOL

Syntax: **#TCSETPAR** EXTERNAL_MEMORY_QSPI_FREQUENCY <Value>

<Value> Accepted parameters are:
- QUAD-SPI
- EXTENDED-SPI
- SPI

Description: Set the SFMC1 protocol used to communicate with SNOR external memory

Note: Default value QUAD-SPI
Available from driver version **5.01**

#TCSETPAR SAMPLING_POINT

Syntax: **#TCSETPAR** SAMPLING_POINT <Value>

<Value> Accepted values are in the range 1-15

Description: Use this parameter to permanently set the sampling point of the FPGA
It is recommended to leave this parameter with the default value

Note: Default value 17

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TELECHIPS TCC Driver Commands

Here you can find the complete list of all available commands for TCC driver.

```
Memory type:

[F] → Program eFlash
[f] → Data eFlash

[N] → Internal NOR flash 2MiB (TCC7045) or 1MiB (TCC7035)
[X] → External NOR flash

[D] → Program eFlash DC Trim
[R] → Program eFlash RED Redundancy
[L] → Program eFlash Logic DC Trim 0 (OTP)
[T] → Program eFlash Logic DC Trim 1 (OTP)
[I] → Program eFlash Information

[d] → Data eFlash DC Trim
[r] → Data eFlash RED Redundancy
[l] → Data eFlash Logic DC Trim 0 (OTP)
[t] → Data eFlash Logic DC Trim 1 (OTP)
[i] → Data eFlash Information
```

#TPCMD CONNECT

#TPCMD CONNECT

This function performs the entry and is the first command to be executed when starting the communication with the device.

```
---#TPCMD CONNECT
Protocol selected JTAG.
Entry Clock is 4.00 MHz.
Trying Reset Impulse connect procedure.
ID-Code read correctly at 4.00 MHz.
JTAG-SWD Debug Port enabled.
Scanning AP map to find all APs.
AP[0] IDR: 0x74770001, Type: AMBA AHB3 bus.
AP[1] IDR: 0x44770002, Type: AMBA APB2 or APB3 bus.
AP[2] IDR: 0x74770001, Type: AMBA AHB3 bus.
Iterating through AP map to find APB-AP to use.
AP[0] Skipped. Not an APB-AP.
AP[1] APB-AP found.
AP[1] ROM table base address 0x80000000.
Iterating through ROM table to find Cortex R5 base address.
 * ROM Table [0][0] Address: 0x80400000 - CID: 0xB105900D - PID: 0x004BBC15.
Found core Cortex R5 with CPU debug base 0x80400000.
Implementer Code: 0x41 - [ARM].
Found core Cortex R5 revision r1p3.
Cortex R5 Core halted [0.001 s].
Requested Clock is 37.50 MHz.
Generated Clock is 37.50 MHz.
Good samples: 3 [Range 6 ~ 8]
ID-Code read correctly at 37.50 MHz.
Configure the internal serial-NOR flash controller.
 * Set SPI peripheral frequency at 85MHz.
 * Maximum 2MiB for code memory extension.
 * SFMC0 serial-NOR flash controller configured.
 * Memory ID: Expected 0x15609D - Read 0x15609D.
 * Detected IS25LP016D memory.
 * Status register 0x40.
 * Set memory status register.
 * Status register 0x00.
 * SFDP table supported.
 * Flash size check passed: 2MiB.
Configure internal serial-NOR memory.
 * Switching from SPI to QUAD-SPI protocol.
 * Set eight dummy cycles.
 * Memory ID: Expected 0x15609D - Read 0x15609D.
 * DDR [Double Data Rate] mode disabled.
 * Use 3-Byte address mode operation.
Time for Connect: 0.126 s.
>|
```


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#TPCMD MASSERASE

#TPCMD MASSERASE <F|X|D|R|I|N|f|d|r|i>
Use this command to erase the Internal NOR memory, External NOR memory, Program eFlash, Program eFlash DC Trim, Program eFlash RED Redundancy, Program eFlash Information, Data eFlash, Data eFlash DC Trim, Data eFlash RED Redundancy or the Data eFlash Information memory.

#TPCMD ERASE

#TPCMD ERASE <F|D|R|I|N|f|d|r|i>
#TPCMD ERASE <F|D|R|I|N|f|d|r|i> <start address> <size>
With this command, a Page Erase of the Program eFlash, Program eFlash DC Trim, Program eFlash RED Redundancy, Program eFlash Information, Data eFlash, Data eFlash DC Trim, Data eFlash RED Redundancy or the Data eFlash Information memory will be performed.
Typically running the Page Erase command takes much longer than running the Masserase command.
Enter the Start Address and Size in hexadecimal format.

#TPCMD BLANKCHECK

#TPCMD BLANKCHECK <F|X|D|R|I|N|f|d|r|i>
#TPCMD BLANKCHECK <F|X|D|R|I|N|f|d|r|i> <start address> <size>
Verify if selected part of the Internal NOR memory, External NOR memory, Program eFlash, Program eFlash DC Trim, Program eFlash RED Redundancy, Program eFlash Information, Data eFlash, Data eFlash DC Trim, Data eFlash RED Redundancy or the Data eFlash Information memory is erased.
Enter the Start Address and Size in hexadecimal format.

#TPCMD PROGRAM

#TPCMD PROGRAM <F|X|D|R|L|T|I|N|f|d|r|l|t|i>
#TPCMD PROGRAM <F|X|D|R|L|T|I|N|f|d|r|l|t|i> <start address> <size>
Program selected part of the Internal NOR memory, External NOR memory, Program eFlash, Program eFlash DC Trim, Program eFlash RED Redundancy, Program eFlash Logic DC Trim 0 (OTP), Program eFlash Logic DC Trim 1 (OTP), Program eFlash Information, Data eFlash, Data eFlash DC Trim, Data eFlash RED Redundancy, Data eFlash Logic DC Trim 0 (OTP), Data eFlash Logic DC Trim 1 (OTP) or the Data eFlash Information memory.
Enter the Start Address and Size in hexadecimal format.

#TPCMD VERIFY

#TPCMD VERIFY <F|X|D|R|L|T|I|N|f|d|r|l|t|i> <R>
#TPCMD VERIFY <F|X|D|R|L|T|I|N|f|d|r|l|t|i> <R> <start address> <size>
R: Readout Mode.
Verify selected part of the Internal NOR memory, External NOR memory, Program eFlash, Program eFlash DC Trim, Program eFlash RED Redundancy, Program eFlash Logic DC Trim 0 (OTP), Program eFlash Logic DC Trim 1 (OTP), Program eFlash Information, Data eFlash, Data eFlash DC Trim, Data eFlash RED Redundancy, Data eFlash Logic DC Trim 0 (OTP), Data eFlash Logic DC Trim 1 (OTP) or the Data eFlash Information memory.
Enter the Start Address and Size in hexadecimal format.

#TPCMD VERIFY <F|X|R|T|I|N|f|d|r|l|t|i> <S>
#TPCMD VERIFY <F|X|R|T|I|N|f|d|r|l|t|i> <S> <start address> <size>
S: Checksum 32 Bit Mode.
Verify selected part of the Internal NOR memory, External NOR memory, Program eFlash, Program eFlash DC Trim, Program eFlash RED Redundancy, Program eFlash Logic DC Trim 1 (OTP), Program eFlash Information, Data eFlash DC Trim, Data eFlash RED Redundancy, Data eFlash Logic DC Trim 0 (OTP), Data eFlash Logic DC Trim 1 (OTP) or the Data eFlash Information memory through Checksum 32Bit method.
Enter the Start Address and Size in hexadecimal format.

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#TPCMD READ

#TPCMD READ <F|X|D|R|L|T|I|N|f|d|r|l|t|i>
#TPCMD READ <F|X|D|R|L|T|I|N|f|d|r|l|t|i> <start address> <size>

Read selected part of the Internal NOR memory, External NOR memory, Program eFlash, Program eFlash DC Trim, Program eFlash RED Redundancy, Program eFlash Logic DC Trim 0 (OTP), Program eFlash Logic DC Trim 1 (OTP), Program eFlash Information, Data eFlash, Data eFlash DC Trim, Data eFlash RED Redundancy, Data eFlash Logic DC Trim 0 (OTP), Data eFlash Logic DC Trim 1 (OTP) or the Data eFlash Information memory.
The result of the read command will be visible into the Terminal.
Enter the Start Address and Size in hexadecimal format.

#TPCMD DUMP

#TPCMD DUMP <F|X|D|R|L|T|I|N|f|d|r|l|t|i>
#TPCMD DUMP <F|X|D|R|L|T|I|N|f|d|r|l|t|i> <start address> <size>

Dump selected part of the Internal NOR memory, External NOR memory, Program eFlash, Program eFlash DC Trim, Program eFlash RED Redundancy, Program eFlash Logic DC Trim 0 (OTP), Program eFlash Logic DC Trim 1 (OTP), Program eFlash Information, Data eFlash, Data eFlash DC Trim, Data eFlash RED Redundancy, Data eFlash Logic DC Trim 0 (OTP), Data eFlash Logic DC Trim 1 (OTP) or the Data eFlash Information memory.
The result of the dump command will be stored in the FlashRunner 2.0 internal memory.
Enter the Start Address and Size in hexadecimal format.

#TPCMD RUN

Syntax: #TPCMD RUN <Time [s]>

<Time [s]> Time in seconds (i.e., 2 s). This time is an optional parameter.

Prerequisites: none

Description: Move the Reset line up and down quickly if no parameter <Time [s]> is inserted.
#TPCMD RUN <Time [s]> instead moves the Reset line down and high, waits for the entered time.
This command typically can be used to execute the firmware programmed in the device.

#TPCMD READ_MEM8

Syntax: #TPCMD READ_MEM8 <Address> <Byte Count>

<Address> Address in HEX format (i.e., 0x52002020)
<Byte Count> Byte count in decimal format (i.e., 8 -> eight bytes)

Prerequisites: none

Description: Read memory byte per byte from target TCC device

Note: This command prints into Terminal and Real Time Log

Examples: Correct command execution: 😊

```
---#TPCMD READ_MEM8 0x52002020 8
Read[0x52002020]: 0xF0
Read[0x52002021]: 0xAA
Read[0x52002022]: 0x16
Read[0x52002023]: 0x14
Read[0x52002024]: 0x00
Read[0x52002025]: 0x00
Read[0x52002026]: 0x00
Read[0x52002027]: 0x00
Time for Read Mem: 0.002 s
```


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#TPCMD READ_MEM16

Syntax: `#TPCMD READ_MEM16 <Address> <16-bit Word Count>`

<Address>	Address in HEX format (i.e., 0x52002020)
<16-bit Word Count>	16-bit Word count in decimal format (i.e., 4 -> four 16-bit words)

Prerequisites: none

Description: Read memory 16-bit word per 16-bit word from target TCC device

Note: This command prints into Terminal and Real Time Log

Examples: Correct command execution: 😊

```
---#TPCMD READ_MEM16 0x52002020 4
Read[0x52002020]: 0xAAF0
Read[0x52002022]: 0x1416
Read[0x52002024]: 0x0000
Read[0x52002026]: 0x0000
Time for Read Mem: 0.002 s
```

#TPCMD READ_MEM32

Syntax: `#TPCMD READ_MEM32 <Address> <32-bit Word Count>`

<Address>	Address in HEX format (i.e., 0x52002020)
<32-bit Word Count>	32-bit Word count in decimal format (i.e., 2 -> two 32-bit words)

Prerequisites: none

Description: Read memory 32-bit word per 32-bit word from target TCC device

Note: This command prints into Terminal and Real Time Log

Examples: Correct command execution: 😊

```
---#TPCMD READ_MEM32 0x52002020 2
Read[0x52002020]: 0x1416AAF0
Read[0x52002024]: 0x00000000
Time for Read Mem: 0.002 s
```

#TPCMD DISCONNECT

`#TPCMD DISCONNECT`

Disconnect function. Power off and exit.

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TELECHIPS TCC Driver Examples

Here you can see a complete example of TELECHIPS TCC projects.

1 – TELECHIPS TCC 4MiB example Commands

TCC7045

```
#TCSETPAR PROTCLK 37500000
#TCSETPAR PWDOWN 100
#TCSETPAR PWUP 100
#TCSETPAR QSPI_FREQUENCY 85MHz
#TCSETPAR QSPI_PROTOCOL QUAD-SPI
#TCSETPAR RSTDOWN 100
#TCSETPAR RSTDRV OPENDRAIN
#TCSETPAR RSTUP 100
#TCSETPAR VPROG0 3300
#TCSETPAR CMODE JTAG
#TPSETSRC 4MiB.frb
#TPSTART
#TPCMD CONNECT
#TPCMD MASSERASE F
#TPCMD BLANKCHECK F
#TPCMD PROGRAM F
#TPCMD VERIFY F R
#TPCMD VERIFY F S
#TPCMD MASSERASE N
#TPCMD BLANKCHECK N
#TPCMD PROGRAM N
#TPCMD VERIFY N R
#TPCMD VERIFY N S
#TPCMD DISCONNECT
#TPEND
```

1 – TELECHIPS TCC 4MiB example Real Time Log

```
---#TPCMD CONNECT
Protocol selected JTAG.
Entry Clock is 4.00 MHz.
Trying Reset Impulse connect procedure.
ID-Code read correctly at 4.00 MHz.
JTAG-SWD Debug Port enabled.
Scanning AP map to find all APs.
AP[0] IDR: 0x74770001, Type: AMBA AHB3 bus.
AP[1] IDR: 0x44770002, Type: AMBA APB2 or APB3 bus.
AP[2] IDR: 0x74770001, Type: AMBA AHB3 bus.
Iterating through AP map to find APB-AP to use.
AP[0] Skipped. Not an APB-AP.
AP[1] APB-AP found.
AP[1] ROM table base address 0x80000000.
Iterating through ROM table to find Cortex R5 base address.
 * ROM Table [0][0] Address: 0x80400000 - CID: 0xB105900D - PID: 0x004BBC15.
Found core Cortex R5 with CPU debug base 0x80400000.
Implementer Code: 0x41 - [ARM].
Found core Cortex R5 revision r1p3.
Cortex R5 Core halted [0.001 s].
Requested Clock is 37.50 MHz.
Generated Clock is 37.50 MHz.
Good samples: 3 [Range 6 ~ 8]
ID-Code read correctly at 37.50 MHz.
Configure the internal serial-NOR flash controller.
 * Set SPI peripheral frequency at 85MHz.
 * Maximum 2MiB for code memory extension.
 * SFMC0 serial-NOR flash controller configured.
 * Memory ID: Expected 0x15609D - Read 0xFFFFFF.
 * Trying to read the Memory ID through QUAD-SPI protocol.
 * Memory ID: Expected 0x15609D - Read 0x15609D.
 * Detected IS25LP016D memory.
 * Status register 0x40.
 * Set memory status register.
 * Status register 0x00.
```


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```
 * SFDP table supported.
 * Flash size check passed: 2MiB.
Configure internal serial-NOR memory.
 * Switching from SPI to QUAD-SPI protocol.
 * Set eight dummy cycles.
 * Memory ID: Expected 0x15609D - Read 0x15609D.
 * DDR [Double Data Rate] mode disabled.
 * Use 3-Byte address mode operation.
Time for Connect: 0.124 s.
>|
---#TPCMD MASSERASE F
Erase matrix 0 [0x20000000 - 0x2007FFFF].
Erase matrix 1 [0x20080000 - 0x200FFFFF].
Erase matrix 2 [0x20100000 - 0x2017FFFF].
Erase matrix 3 [0x20180000 - 0x201FFFFF].
Time for Masserase F: 0.033 s.
>|
---#TPCMD BLANKCHECK F
Time for Blankcheck F: 0.365 s.
>|
---#TPCMD PROGRAM F
Time for Program F: 3.591 s.
>|
---#TPCMD VERIFY F R
Time for Verify Readout F: 0.952 s.
>|
---#TPCMD VERIFY F S
Time for Verify Checksum 32bit F: 0.168 s.
>|
---#TPCMD MASSERASE N
Time for Masserase N: 3.692 s.
>|
---#TPCMD BLANKCHECK N
Time for Blankcheck N: 0.295 s.
>|
---#TPCMD PROGRAM N
Time for Program N: 0.871 s.
>|
---#TPCMD VERIFY N R
Time for Verify Readout N: 0.867 s.
>|
---#TPCMD VERIFY N S
Time for Verify Checksum 32bit N: 0.137 s.
>|
---#TPCMD DISCONNECT
>|
```

1 – TELECHIPS TCC 4MiB example Programming Times

Operation	Timings FlashRunner 2.0
Time for Connect	0.124 s
Masserase *Program eFlash 2MiB*	0.033 s
Blankcheck *Program eFlash 2MiB*	0.365 s
Program *Program eFlash 2MiB*	3.591 s
Verify Readout *Program eFlash 2MiB*	0.952 s
Verify Checksum *Program eFlash 2MiB*	0.168 s
Masserase *Internal SNOR 2MiB*	3.692 s
Blankcheck *Internal SNOR 2MiB*	0.295 s
Program *Internal SNOR 2MiB*	0.871 s
Verify Readout *Internal SNOR 2MiB*	0.867 s
Verify Checksum *Internal SNOR 2MiB*	0.137 s
Cycle Time	**00:11.157 s**

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TELECHIPS TCC Driver Changelog

Info about driver version 5.00 - 17/12/2024
First official version for TCC driver.
Supported TELECHIPS TCC7x series.

Info about driver version 5.01 - 18/03/2025
Supported flashing an external memory through TCC7045 device using SPI peripheral.

SMH Technologies S.r.l.

UNIVERSAL PRODUCTION IN-SYSTEM PROGRAMMING

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